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10/081,190	02/25/2002	Hirofumi Sudo	8040-1001	2766

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/081,190	Applicant(s) SUDO ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-174* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,4,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because some of the characters and symbols in the drawings are difficult to read due to the poor quality of the faxed drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to 0the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 's20' in

Figure 4. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because numeral references to the figures must be removed. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshimi; Susumu et al. (US 4446490 A, hereafter referred to as Hoshimi490) in view of Hoshimi; Susumu et al. (US 4404602 A, hereafter referred to as Hoshimi602).

35 U.S.C. 103(a) rejection of claims 1 and 10.

Hoshimi490 teaches an output driver connected to said first processor unit for transmitting said intercommunicating signals supplied from a processor unit in the form of a serial signal having a redundancy data structure (Figure 1 of Hoshimi490 is an output driver comprising error correction circuitry for use in a PCM processor unit for transmitting said intercommunicating signals supplied from said PCM processor unit to a recording medium in the form of a serial signal having a redundancy data structure); and an input driver connected to said output driver and said second processor unit for receiving said serial signal transmitted from said output driver to reproduce said intercommunicating signals in the form of parallel signals and to supply the reproduced intercommunicating signals to said second processor unit (Figure 3 of Hoshimi490 is an input driver connected to said output driver in Figure 1 of Hoshimi490 and a PCM

processor unit for receiving said serial signal transmitted from said output driver in Figure 1 to reproduce said intercommunicating signals in the form of parallel signals and to supply the reproduced intercommunicating signals to said PCM processor unit). However Hoshimi490 does not explicitly teach the specific use of two separate processing units for transmitting and receiving, i.e. for recording and reproducing. Hoshimi602, in an analogous art, teaches separate PCM processors for a VTR recording apparatus, one for transmitting said intercommunicating signals supplied from said PCM processor unit to a recording medium and the second PCM processor for receiving said serial signal transmitted from said output driver to reproduce said intercommunicating signals in the form of parallel signals and to supply the reproduced intercommunicating signals to said PCM processor unit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hoshimi490 with the teachings of Hoshimi602 by including use of two separate processing units for transmitting and receiving, i.e. for recording and reproducing. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of two separate processing units for transmitting and receiving, i.e. for recording and reproducing would have provided the opportunity to provide error correction in the VTR device of Hoshimi602 for which it was designed.

4. Claims 2-8 and 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshimi; Susumu et al. (US 4446490 A, hereafter referred to as Hoshimi490) and Hoshimi; Susumu et al. (US 4404602 A, hereafter referred to as Hoshimi602) in view of Kojima; Tadashi (US 4459696 A).

35 U.S.C. 103(a) rejection of claims 2 and 11.

Hoshimi490 and Hoshimi602 substantially teach the claimed invention described in claim 1 (as rejected above). In addition Hoshimi490 teaches that the output driver Figure 1 of Hoshimi490 comprises a coding circuit (P.Q Encoder 4 and CRCC Adder 7 in Figure 1) for producing an error detecting code signal as said serial signal and input driver Figure 3 of Hoshimi490 comprises an decoding circuit for decoding said error detecting code signal to detect an error on said error detecting code signal (CRCC Detector 11 and Error Correction Circuit 15 in Figure 9; Note: CRC codes are inherently capable of detecting correctable and uncorrectable errors).

However Hoshimi490 and Hoshimi602 do not explicitly teach the specific use of suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected.

Kojima, in an analogous art, teaches that if there are too many errors for the error correction circuitry, i.e., if an uncorrectable error is detected, supply of the reproduced intercommunicating signal is suspended and in favor of error compensated data provided by error compensator 29 in Figure 7 of Kojima (col. 6, lines 12-17, Kojima).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hoshimi490 and Hoshimi602 with the teachings of Kojima by including use of suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of suspending supply of said reproduced intercommunicating signals to said second processor unit when said error is detected would have provided the opportunity to establish a better compensated estimate of erroneous audio data.

35 U.S.C. 103(a) rejection of claims 3 and 12.

Hoshimi490, Hoshimi602 and Kojima teach a redundancy bit producing circuit connected to said first processor unit for producing at least one redundancy bit on the basis of said intercommunicating signals (CRCC Adder 7 in Figure 1 of Hoshimi490 is a redundancy bit producing circuit connected to said first processor unit for producing CRC redundancy bits on the basis of said intercommunicating signals), and a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bits in a predetermined cycle to produce said serial signal (Parallel to Serial Converter 6 in Figure 1 of Hoshimi490 is a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bits in a predetermined cycle to produce said serial signal), said decoding circuit comprising: a demultiplexing circuit

connected to said multiplexing circuit for demultiplexing said serial signal into received intercommunicating signals and received redundancy bits (Serial to Parallel Converter 12 in Figure 3 of Hoshimi490 is a demultiplexing circuit connected to said multiplexing circuit for demultiplexing said serial signal into received intercommunicating signals and received redundancy bits), a error detecting circuit connected to said demultiplexing circuit for detecting an error on said received intercommunicating signals by the use of said received redundancy bits (CRCC Detector 11 in Figure 3 of Hoshimi490 is a error detecting circuit connected to said demultiplexing circuit for detecting an error on said received intercommunicating signals by the use of said received CRC redundancy bits), and a signal holding circuit connected to said error detecting circuit and said second processor unit for holding said received intercommunicating signals to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit (Interleaver 14 in Figure 3 of Hoshimi490 is a signal holding circuit connected to said error detecting circuit and said second processor unit for holding said received intercommunicating signals to supply said received intercommunicating signals as said reproduced intercommunicating signals to said second processor unit).

35 U.S.C. 103(a) rejection of claims 4 and 13.

Hoshimi490, Hoshimi602 and Kojima teach that said error detecting circuit clears held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit when an uncorrectabe error is

detected (Kojima, in an analogous art, teaches that if there are too many errors for the error correction circuitry, i.e., if an uncorrectable error is detected, supply of the reproduced intercommunicating signal is suspended and in favor of error compensated data provided by error compensator 29 in Figure 7 of Kojima; see col. 6, lines 12-17, Kojima).

35 U.S.C. 103(a) rejection of claims 5, 6, 14 and 15.

CRC is parity (CRCC Adder 7 in Figure 1 of Hoshimi490).

35 U.S.C. 103(a) rejection of claims 7 and 16.

Parallel to Serial Converter 6 in Figure 1 of Hoshimi490 is a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bits in a predetermined cycle to produce said serial signal. Timing signals are inherently required to operate a Parallel to Serial Converter for pulsed digital data.

35 U.S.C. 103(a) rejection of claims 8 and 17.

Hoshimi490, Hoshimi602 and Kojima said decoding circuit further comprises a timer circuit connected to demultiplexing circuit and said signal holding circuit (Parallel to Serial Converter 6 in Figure 1 of Hoshimi490 is a multiplexing circuit connected to said redundancy bit producing circuit for multiplexing said intercommunicating signals and said redundancy bits in a predetermined cycle to produce said serial signal; timing

signals are inherently required to operate a Parallel to Serial Converter for pulsed digital data) for clearing held content held in said signal holding circuit to suspend supply of said reproduced intercommunicating signals to the second processor unit (Kojima, in an analogous art, teaches that if there are too many errors for the error correction circuitry, i.e., if an uncorrectable error is detected, supply of the reproduced intercommunicating signal is suspended and in favor of error compensated data provided by error compensator 29 in Figure 7 of Kojima; see col. 6, lines 12-17, Kojima) when said demultiplexing circuit does not receive said serial signal for a predetermined time period (col. 7, line 32-38 in Kojima teaches that error compensation is used for drop-out errors; Note: a drop-out errors include complete failures to receive a signal within a reasonable amount of time).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoshimi; Susumu et al. (US 4446490 A, hereafter referred to as Hoshimi490) and Hoshimi; Susumu et al. (US 4404602 A, hereafter referred to as Hoshimi602) in view of Camiciottoli; Roberto et al. (US 3760127 A, hereafter referred to as Camiciottoli).

35 U.S.C. 103(a) rejection of claim 9.

Hoshimi490 and Hoshimi602 substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hoshimi490 and Hoshimi602 do not explicitly teach the specific use of an additional output driver connected to said second processor unit and having the same

structure as said output driver for transmitting additional intercommunicating signals supplied from said second processor unit; and an additional input driver connected to said additional output driver and said first processor unit and having the same structure as said input driver for reproducing said additional intercommunicating signals to supply the reproduced additional intercommunicating signals to said first processor unit.

Camiciottoli, in an analogous art, teaches repeaters in a PCM intercommunication system for transmitting PCM data whereby each repeater is a transceiver comprising a processor for receiving, monitoring and transmitting PCM data.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hoshimi490 and Hoshimi602 with the teachings of Camiciottoli by including use of an additional output driver connected to said second processor unit and having the same structure as said output driver for transmitting additional intercommunicating signals supplied from said second processor unit; and an additional input driver connected to said additional output driver and said first processor unit and having the same structure as said input driver for reproducing said additional intercommunicating signals to supply the reproduced additional intercommunicating signals to said first processor unit. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of an additional output driver connected to said second processor unit and having the same structure as said output driver for transmitting additional intercommunicating signals supplied from said second processor unit; and an additional input driver connected to said additional output driver and said

first processor unit and having the same structure as said input driver for reproducing said additional intercommunicating signals to supply the reproduced additional intercommunicating signals to said first processor unit would have provided the opportunity to provide error protection for repeaters in a PCM intercommunication system.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Art Unit 2133